WHAT IS CLAIMED IS:

1. A method for processing digital video signals for live video applications, the method comprising:

providing video data comprising a plurality of frames;

identifying a first frame and a second frame in the frame sequences;

processing the information of the first frame and the information of the second frame to determine a quantization step value for the second frame;

adjusting a transmission bit rate for the second frame in response to the quantization step value.

2. The method of claim 1 wherein the providing video data comprises:

assigning compression modes to the frames.

3. The method of claim 2 wherein the compression modes are selected from a group comprising I-mode, P-mode, and B-mode.

4. The method of claim 1 wherein the processing the information of the first frame and the information of the second frame comprises:

calculating a sigmaSAD value for the second frame;

calculating a divisor value for the second frame;

calculating the quantization step for the second frame.

5. The method of claim 4 wherein the calculating a sigmaSAD value comprises:

calculating a SAD value for each microblock of the second frame;

storing the SAD value in a memory unit for each microblock of the second frame;

calculating the sum of all the SAD values for the second frame;

dividing the sum by the total number of microblocks of the second frame.

6. The method of claim 4 wherein the calculating a divisor value comprises

selecting a series of integers that is indexed from 0 through n-1;

selecting a complexity integer;

calculating the quotient modulo n of the complexity integer;

setting the divider value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

7. The method of claim 6 wherein the selecting a complexity integer comprises:

if the second frame is an I-frame, setting the complexity integer near midrange between an integer A and an integer B;

if the second frame is not an I-frame, adjusting the complexity integer so that the fullness of a buffer varies toward a predefined fullness level.

8. The method of claim 4 wherein the calculating the quantization step comprises setting the quantization step equal to the sum of the ratio of the sigmaSAD value to the divisor value, and a constant.

9. The method of claim 8 wherein the constant equals 1.

10. The method of claim 1 wherein the processing the information of the first frame and the information of the second frame comprises:

deciding whether to encode a frame in the I-mode before any P-frame encoding is accomplished.

11. The method of claim 6 wherein the processing comprises:

Adjusting the complexity integer so that the size of encoded data for anyone of the plurality of frames has approximately an equal size.

12. The method of claim 1 wherein the method for processing digital video signals further comprises:

determining the locations of I-frames in the step of providing video data;

extending frames immediately preceding the I-frames for one additional frame time;

skipping frames immediately following the I-frames.

13. A system including a processor for processing digital video signals for live video applications, the system comprising:

a memory unit within which a computer program is stored, the computer program comprising:

code that instructs the processor to receive video data comprising a plurality of frames;

code that directs the processor to identify a first frame and a second frame in the frame sequences;

code that directs the processor to process the information of the first frame and the information of the second frame to determine a quantization step for the second frame.

14. The system of claim 13 wherein the code that directs the processor to process the information of the first frame and the information of the second frame comprises:

code that calculates a sigmaSAD value for the second frame;

code that calculates a divisor value for the second frame;

code that calculates the quantization step for the second frame.

15. The code of claim 14 that calculates a sigmaSAD value comprises:

code that calculates a SAD value for each microblock of the second frame;

code that stores the SAD value in a memory unit for each microblock of the second frame;

code that calculates the sum of all the SAD values for the second frame;

code that divides the sum by the total number of microblocks of the second frame.

16. The code of claim 14 that calculates a divisor value comprises

code that selects a series of integers that is indexed from 0 through n-1;

code that selects a complexity integer;

code that calculates the quotient modulo n of the complexity integer;

code that sets the divider value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

17. The code of claim 16 that selects a complexity integer comprises:

code that sets the complexity integer near midrange between an integer A and an integer B if the second frame is an I-frame;

code that adjusts the complexity integer so that the fullness of a buffer varies toward a predefined fullness level if the second frame is not an I-frame.

18. A system for processing digital video signals for live video applications, the system comprising:

a video providing subsystem that provides video data comprising a plurality of frames;

a sigmaSAD calculation subsystem that calculates a value of sigmaSAD;

a divisor calculation subsystem that calculates a value of divisor.

19. The system of claim 18 wherein the sigmaSAD calculation subsysterm comprises:

a subsystem that calculates a SAD value for each microblock of a frame of the plurality of frames;

a subsystem that stores the SAD value in a memory unit for each microblock of the frame;

a subsystem that calculates the sum of all the SAD values for the frame;

a subsystem that divides the sum by the total number of microblocks of the frame.

20. The system of claim 18 wherein the divisor calculation subsystem comprises

a subsystem that selects a series of integers that is indexed from 0 through n-1;

a subsystem that selects a complexity integer;

a subsystem that calculates the quotient modulo n of the complexity integer;

a subsystem that sets the divider value equal to an integer whose index in the series equals the quotient;

wherein n is an integer larger than 1.

21. The subsystem of claim 20 that selects a complexity integer comprises:

a subsystem that if the second frame is an I-frame, sets the complexity integer near midrange between an integer A and an integer B;

a subsystem that if the second frame is not an I-frame, adjusts the complexity integer so that the fullness of a buffer varies toward a predefined fullness level.

22. The system of claim 18 further comprises:

a quantization step calculation subsystem that sets the quantization step equal to the sum of the ratio of the value of sigmaSAD to the value of divisor, and a constant.